



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

16

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.												
10/811,811	03/30/2004	Yasuhiro Takeda	57810-095	2835												
7590 McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096		<table border="1"><tr><td colspan="2">EXAMINER</td></tr><tr><td colspan="2">LANDAU, MATTHEW C</td></tr><tr><td>ART UNIT</td><td>PAPER NUMBER</td></tr><tr><td colspan="2">2815</td></tr><tr><td>MAIL DATE</td><td>DELIVERY MODE</td></tr><tr><td colspan="2">05/22/2007 PAPER</td></tr></table>			EXAMINER		LANDAU, MATTHEW C		ART UNIT	PAPER NUMBER	2815		MAIL DATE	DELIVERY MODE	05/22/2007 PAPER	
EXAMINER																
LANDAU, MATTHEW C																
ART UNIT	PAPER NUMBER															
2815																
MAIL DATE	DELIVERY MODE															
05/22/2007 PAPER																

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/811,811	TAKEDA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

- 1) Responsive to communication(s) filed on 08 March 2007.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

- 4) Claim(s) 1-8,18-31 and 36-38 is/are pending in the application.
- 4a) Of the above claim(s) 18-30 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-8,31 and 36-38 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

**DETAILED ACTION**

***Election/Restrictions***

Claims 18-30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse in the reply filed December 29, 2005.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

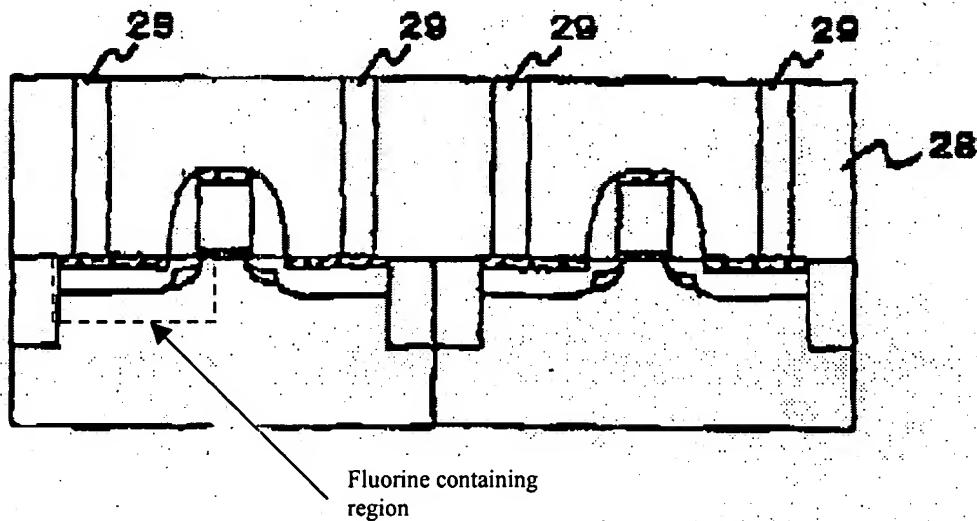
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 8, 31, and 36-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. (US Pat. 6,436,783, hereinafter Ono).

Regarding claims 1, 3-5, 36, and 37, Figures 1-4 and 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); an element isolation region 2 isolating an active region; a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7; and side wall insulator films 18 (silicon oxide) (col. 21, lines 53-55) formed on the side surfaces of said gate electrode. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-

Art Unit: 2815

12). The channel region extends over a junction interface between the source/drain regions (16/22) and the substrate 1. Therefore, Figures 1-4 of Ono disclose a fluorine containing region (see below figure) extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain region. It is considered that "a region" is an arbitrary region/area extending from the isolation region including the source/drain region and the channel, as shown in the below figure. Since the fluorine is at least in the channel, the fluorine is in the claimed region. Note that the claim does not require fluorine to be in every part of the region.



Regarding claims 2, 7, and 8, Ono also discloses fluorine is present in the interface between the gate insulator film and the central region of said channel region (col. 21, lines 38-41) as well as said gate insulator film 7. Note that Ono discloses the amount of fluorine introduced into the gate insulator is reduced and that "almost" no fluorine is in the gate insulator

Art Unit: 2815

film (col. 8, lines 16-18 and 48-50). Therefore, there is at least some fluorine in the gate insulator film. Further regarding claims 2 and 7, Ono also discloses the sidewalls can be formed prior to the fluorine implantation (col. 16, lines 49-51). Therefore, it would be inherent that at least some fluorine is introduced into the side wall insulator films during the implantation step.

Regarding claims 31 and 38, Figures 1-4 and 7-9 of Ono disclose a semiconductor device comprising: a first conductivity type semiconductor region (silicon substrate 1) (col. 11, lines 63-65) having a main surface (upper surface); an element isolation region 2 isolating an active region; a second conductivity type source/drain region (16/22) formed on said main surface to hold a channel region therebetween at a prescribed interval; a gate electrode 20 formed on said channel region through a gate insulator film 7; and side wall insulator films 18 (silicon oxide) (col. 21, lines 53-55) formed on the side surfaces of said gate electrode. Ono discloses fluorine has been introduced into the channel region (col. 13, lines 10-12). The channel region extends over a junction interface between the source/drain regions (16/22) and the substrate 1.

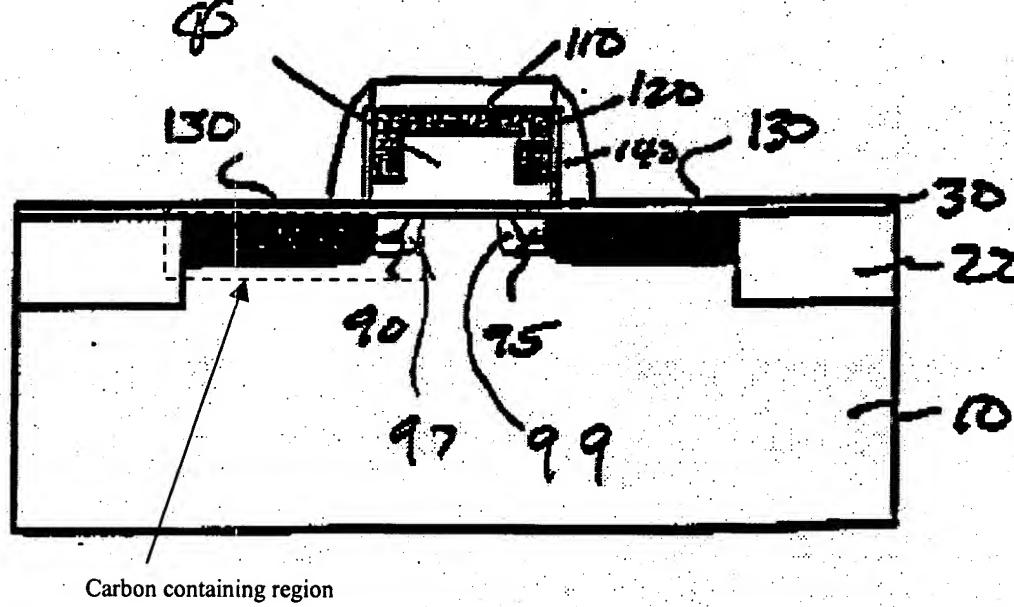
Therefore, Figures 1-4 of Ono disclose a fluorine containing region (see above figure) extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type source/drain region. It is considered that "a region" is an arbitrary region/area extending from the isolation region including the source/drain region and the channel, as shown in the below figure. Since the fluorine is at least in the channel, the fluorine is in the claimed region. Note that the claim does not require fluorine to be in every part of the region. Ono also discloses fluorine is present in the interface between the gate insulator film and the central region of said channel region (col. 21, lines 38-41) as well as said gate insulator film 7. Note that Ono discloses the amount of fluorine

introduced into the gate insulator is reduced and that “almost” no fluorine is in the gate insulator film (col. 8, lines 16-18 and 48-50). Therefore, there is at least some fluorine in the gate insulator film. Furthermore, Ono discloses the sidewalls can be formed prior to the fluorine implantation (col. 16, lines 49-51). Therefore, it would be inherent that at least some fluorine is introduced into the sidewall insulator films during the implantation step.

Claims 1, 3, 5, 6, 36, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandelman et al. (US PGPub 2003/0020125, hereinafter Mandelman).

Regarding claims 1, 5, 36, and 37, Figure 10 of Mandelman discloses a semiconductor device comprising: a first conductivity type semiconductor region (well region in substrate 10) (paragraph [0047]) having a main surface; an element isolation region 20 isolating an active region; a second conductivity type impurity region (90/95/130) formed on said main surface of said semiconductor region to hold a channel region therebetween at a prescribed interval; a carbon containing region (area including regions 97/99, see below figure) extending from the element isolation region over a junction interface between said first conductivity type semiconductor region and said second conductivity type impurity region (paragraph [0050]); a gate electrode 80 formed on said channel region through a gate insulator film; and side wall insulator films 140 formed on the side surfaces of said gate electrode. It is considered that “a region” is an arbitrary region/area extending from the isolation region including the source/drain region and the halo implant (see below figure). Since the carbon is in the area beneath the gate, carbon has been introduced into the claimed region. Note that the claim does not require carbon

to be in every part of the region. Furthermore, the phrase, "extending from" does not necessarily mean the carbon containing region is in contact with isolation region. Therefore, regions 97 and 99 by themselves could alternatively be considered to read on the claimed carbon containing region, since they extend in a horizontal direction away from the isolation regions.



Regarding claim 3, Mandelman discloses the substrate 10 is formed of silicon (paragraph [0043]). Therefore, said first conductivity type semiconductor region includes a first conductivity type silicon region.

Regarding claim 6, Figure 10 of Mandelman discloses said impurity region (90/95/130) includes a low-concentration impurity region (90/95) (LDD regions) (paragraph [0050]) and a

high concentration impurity region 130 (source/drain region), and said element of carbon is introduced into at least a region (97/99) extending over the junction interface between said first conductivity type semiconductor region and said high-concentration impurity region. Note that Figure 10 shows regions 97 and 99 extend over a part of the junction interface between the source/drain regions 130 and the substrate.

*Response to Arguments*

Applicant's arguments filed December 8, 2006 have been fully considered but they are not persuasive.

Applicant argues that Ono does not disclose a region containing fluorine or carbon extending from an element isolation region as claimed and that "since Ono et al. describe introducing fluorine "into the channel region," it is apparent that the channel region does not extend from field oxide film 2 (element isolation region)." As explained in the above rejection, "a region" can be considered an arbitrarily defined area extending from the isolation region. A figure has been provided in the body of the above rejection to further illustrate this point. It has been considered that "a region" is an arbitrary area extending from the isolation region including the source/drain region and the channel. Since fluorine is in at least in the channel, fluorine is in the "region". Applicant has not explicitly defined the term "region" in a manner that would preclude this interpretation, nor do the claims require fluorine to be in every part of the claimed region. Further, the phrase "extending from" does not necessarily mean the fluorine or carbon

containing region is in contact with isolation region. "Extending from the element isolation region" could simply mean the isolation region is a point of reference from which the fluorine or carbon containing region extends, not that the isolation region is necessarily the starting point from which the fluorine or carbon containing region extends. Since the channel extends in a horizontal direction, it can be considered to extend from isolation region. Note that Applicant makes similar arguments regarding Mandelman and the above response equally applies.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

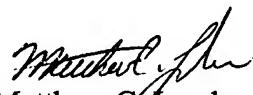
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2815

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is 571-272-1731. The examiner can normally be reached on 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Matthew C. Landau  
Primary Examiner  
Art Unit 2815

5/16/07